COMMUNICATIONS SIGNAL AMPLIFIERS HAVING INDEPENDENT POWER CONTROL AND AMPLITUDE MODULATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to communications signal amplifiers and to power control and amplitude modulation control.

2. State of the Art

High linearity and high energy efficiency are two principal (and usually competing) objectives of conventional communications signal amplifier design. High linearity is required to produce "clean" communications signals that produce a minimum of interference and provide high quality of service. High energy efficiency is desirable particularly for portable, battery-powered devices, as well as for purposes of reducing infrastructure costs.

In a cellular telecommunications system, handsets and other devices communicating with the radio base station are required to transmit at one of many possible power levels depending on the proximity of a particular device to the base station. This average output power control function may for some standards entail a dynamic range of 80dB. Achieving linearity over this wide dynamic range has proved problematic.

Referring to Figure 1, a simplified diagram of a conventional communications signal transmitter is shown. A signal generator 101 generates a signal having both amplitude and phase modulation. This signal is applied to an amplitude varying circuit 103 such as a variable gain amplifier (VGA) or variable attenuator controlled in accordance with a power level signal 104. A resulting scaled signal is then applied to a linear amplifier 105 to achieve final amplification. In this arrangement, because the amplitude-modulated signal passes through the amplitude varying circuit 103, the amplitude varying circuit must have very linear performance.

An alternate approach involves polar modulation, in which separate ampli-

tude and phase paths are provided. Polar modulation architectures (and similar architectures in which separate amplitude and phase paths are provided) are described, for example, in U.S. Patents 6,191,653, 6,194,963, 6,078,628, 5,705,959, 6,101,224, 5,847,602, 6,043,707, and 3,900,823, as well as French patent publication FR 2768574, all of which are incorporated herein by reference.

Referring in particular to U.S. Patent 6,191,653, an RF power amplifier architecture is described in which separate phase and amplitude paths are provided. The amplifier has multiple stages. For signals having a comparatively high average power level, amplitude modulation is achieved in a final amplifier stage operating in a non-linear mode. In the case of a FET (field effect transistor) active device, for example, drain modulation is applied to the FET in order to impress the desired amplitude modulation upon the output signal. For signals having a low average power level, amplitude modulation is achieved in a preceding amplifier stage (again using drain modulation), the final amplifier stage being operated in linear mode (see column 6). In this manner, a range of amplitude modulation is provided that is larger than can be supported by just drain modulation of the final stage. Achieving an 80dB dynamic range of average output power using this arrangement, however, remains problematic. Furthermore, any non-linearities in amplitude modulation performed in the driver stage are magnified in the final stage.

The present invention addresses the need for wide dynamic range of average output power without requiring high linearity. When applied in conjunction with switch mode amplification techniques, overall high efficiency may be achieved.

SUMMARY OF THE INVENTION

The present invention, generally speaking, provides methods and apparatus for producing an amplitude modulated communications signal, in which a constant-envelope carrier signal is modified in response to a power control signal to

produce a modified constant-envelope carrier signal. The modified constant-envelope carrier signal is amplified in response to an amplitude modulation signal to produce a communications signal having amplitude modulation and having an average output power proportional to a signal level of the modified constant-envelope carrier signal. This manner of operation allows wide dynamic range of average output power to be achieved. Because amplitude modulation is applied after amplitude varying circuitry used to produce the modified constant-envelope carrier signal, the amplitude modulation is unaffected by possible non-linearities of such circuitry. In accordance with another aspect of the invention, operation in the foregoing manner at comparatively low average output power levels is combined with switch mode operation at comparatively high average output power levels, enabling high overall efficiency to be achieved. Hence, the disclosed modulator and amplifier combination, in addition to supporting very low power signals, also supports high power signals.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a simplified diagram of a conventional communications signal amplifier;

Figure 2 is a simplified diagram of a communications signal amplifier in accordance with the principles of the present invention;

Figure 3 is a diagram of a communications signal amplifier like that of Figure 2 showing one particular amplification chain;

Figure 4 is a block diagram of a communications transmitter in which the present invention may be used;

Figure 5 is a more detailed diagram of the amplification chain of the power amplifier of Figure 4, in accordance with an exemplary embodiment;

Figure 6 is a plot of device characteristics for the amplifier section of Figure 5;

Figure 7 is a more detailed block diagram of portions of one embodiment of the communications transmitter of Figure 4;

Figure 8 is a block diagram of another embodiment of the communications transmitter;

Figure 9 is a more generalized block diagram of the present communications signal transmitter;

Figure 10 is a plot illustrating high power switch-mode operation;

Figure 11 is a plot illustrating operation of a conventional amplifier;

Figure 12 is a plot illustrating low power switch-mode operation;

Figure 13 is a plot illustrating very low power, multiplicative-mode operation;

Figure 14 is a plot like that of Figure 13, showing the boundary of a 5% linearity region;

Figure 15 is a spectrum plot of an EDGE signal at 30 dBm; and

Figure 16 is a spectrum plot of the same EDGE signal at -50 dBm.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 2, there is shown a simplified diagram of a communications signal amplifier in accordance with the principles of the present invention. A signal generator 201 generates a signal typically (though not necessarily) having phase information. This signal is applied to an amplitude varying circuit 203 such as a variable gain amplifier (VGA) or an attenuator, controlled in accordance with a power level signal 204. A resulting scaled signal is then applied to an amplification chain 205. The amplification chain is responsive to a control signal 207 bearing amplitude modulation information (and possibly power level information in addition to that of the power level signal 204) to produce an amplified communications signal (e.g., RF output signal) having the desired amplitude modulation and desired power level.

Figure 3 shows further details of the communications signal amplifier of Figure 2, particularly of the amplification chain. In the illustrated embodiment, the

amplification chain is shown as having a single final amplifier stage 307 operating in multiplicative mode to achieve both amplitude modulation and final amplification or, at low power levels, attenuation, as the case may be. The final amplifier stage includes a three-terminal active device Q (such as an FET) having a signal input terminal IN, an output terminal OUT and a power supply input terminal PS. An amplitude modulation signal 307 is applied to the power supply input terminal. In this arrangement, because the amplitude-modulated signal does not pass through the amplitude varying circuit 303, the amplitude varying circuit may have non-linear performance. To the extent the non-linear characteristics of the amplitude varying circuit 303 may be ascertained, they may be taken compensated for in setting the power level signal 304 applied to the amplitude varying circuit.

Optionally, power level control, instead of being applied to the final amplifier stage solely through the signal input path IN, may be applied in combination through both the signal input path and the power supply path PS.

The amplitude varying circuit 303 may be a variable gain amplifier (VGA) or a variable attenuator, controlled in accordance with a power level signal. The VGA or variable attenuator may be realized in one stage or several stages, using passive devices, active devices, or some combination of the same, where the active devices (if any) are operated in either "triode mode" or switch mode.

Referring to Figure 4, a block diagram is shown of a communications transmitter in which the present invention may be used. A data signal 401 is applied to a control block 403, such as a DSP, ASIC, ASSP, etc. In the general case, the control block produces a number of control signals, one or more of which are applied to each of a DDS/phase control block 405 (where DDS stands for direct digital synthesis) and an amplitude/power control block 407. In a specific embodiment, as described below, the control block 403 produces a single phase control signal and multiple amplitude control signals.

An output signal of the DDS/phase control block 405 is applied to the

amplitude/power control block 407. Responsive to the output signal of the DDS/phase control block 405 and to control signal(s) from the control block 403, the amplitude/power control block 407 produces a signal output and a power supply output that are applied to a signal input 409 and a power supply input 411, respectively, of an amplification chain 413 (shown in simplified form). The amplification chain 413 has at least one amplification stage 413a and typically two or more amplification stages, as indicated in dashed lines, and amplifies the signal input 409 to produce an amplified communications signals such as an RF output signal, RF OUT.

The amplification chain of Figure 4 may, in some embodiments, be operated exclusively in "triode mode" or "multiplicative mode" (described more fully below), as opposed to switch mode, across the entire output signal dynamic range. In triode mode, with the active device operating in the triode region, average output power increases with increase of the signal input level and with increase of the power supply input level. Hence, for maximum average output power, levels of the signal input level and the power supply input would be set to maximum levels subject to the requirement of operating the amplifier in multiplicative mode. Similarly, for minimum average output power, levels of the signal input level and the power supply input would be set to minimum levels subject to the requirement of operating the amplifier in multiplicative mode.

When operated this manner, power efficiency, while not especially high, is improved as compared to more conventional amplifiers in which the power supply input to the amplifier is held fixed. However, amplifier performance is somewhat sensitive to manufacturing and environmental influences. Increased power efficiency and dramatically decreased sensitivity to manufacturing and environmental influences may be achieved by operating the amplification chain, during at least part of the time, in switch mode.

Referring to Figure 5, a more detailed diagram of the amplification chain of

the power amplifier of Figure 4 is shown, in accordance with an exemplary embodiment. The amplification chain is shown as having three stages, each stage including an active power device. The active devices are illustrated here as FETs (Field Effect Transistors) Q1, Q2 and Q3, but can be any three-terminal gain device. In the illustrated embodiment, the drain terminals of the FETs are each connected through a respective inductive choke, L1, L2 and L3, to a respective power supply input, VDD1, VDD2, VDD3. Hence, the power supply inputs of the three devices may be controlled independently. The source terminals of the active device are coupled to a reference potential, e.g., ground.

A signal input is applied to a gate terminal of the first active device Q1, which produces an output signal at the drain terminal thereof. This output signal is applied to a coupling network CN1 that produces a signal input for the second active device, Q2, which is applied to the gate terminal thereof. Similarly, the output signal produced at the drain of the second active device Q2 is applied to a coupling network CN2 that produces a signal input for the third active device Q3. Note that a parasitic capacitance, CGD, exists between the gate and drain of each of the active devices. This capacitance gives rise to a signal leakage phenomenon that has heretofore made the achievement of very wide dynamic range on the output signal of the amplification chain problematic.

The output signal produced by the third active device Q3 is AC-coupled through a capacitor to a load network. An RF output signal is developed across the load network and may be transmitted, for example by an antenna.

In operation of the amplification chain of Figure 5, drain modulation is performed by applying an amplitude modulation signal to one or more of the drain supplies (VDD1, VDD2, VDD3) while driving the signal input at a high level to drive at least the final amplifier stage, and preferably all the amplifier stages, into deep compression or switch mode. When the final amplifier stage is overdriven in this manner, the power of the RF output signal developed across the load network is

proportional to the square of the supply voltage on the terminal VDD3.

A normal mode of operation (as described, for example, in the above U.S. Patent 6,191,653 in relation to a first embodiment thereof) would be to modulate the power supply input of the final stage (i.e., VDD3) and to operate the power supply inputs of preceding stages (i.e., VDD1, VDD2) at a fixed voltage. In this mode of operation, modulation of the power supply input VDD3 may require a voltage swing ratio of 8:1 for signals such at that used in the EDGE system.

Where it is required that the RF output power be varied over a wide range of power levels (e.g., 80dB dynamic range), some of this dynamic range may be achieved by scaling down the applied amplitude modulation signal, i.e., by increasing its dynamic range. This method, however, is limited by feed-through of the Q3 input signal to the output via the capacitor CGD3. Leakage of the input signal to the output signal causes AM to AM and AM to PM non-linearities at low levels of the power supply input VDD3.

As described in co-pending application 09/684,497 entitled POWER CONTROL AND MODULATION OF SWITCH MODE POWER AMPLIFIERS WITH ONE OR MORE STAGES, filed on October 6, 2000 and incorporated herein by reference, the foregoing problem may be alleviated by reducing the power supply input levels VDD2 and/or VDD1, to minimize feed-through due to the capacitor(s) CGD. This technique has been shown to achieve an output power dynamic range of 40dB or more, considerably short of the 80dB desired for some cellular applications. A different approach is need to achieve this extended dynamic range. Such an approach may be based on the following observations.

When operating at low power levels corresponding to supply voltages of less than 1V (e.g., a few or several tenths of a volt), the amplifier stages may no longer operate in non-linear mode, if the RF input drive to a stage is reduced sufficiently so that it is no longer of sufficient magnitude to overcome the DC bias of that stage to turn it OFF. (For example, if the DC bias were set to -2V, and the FET

threshold were -2.5V, any RF signal with magnitude 0.5V or less would not achieve the -2.5V necessary to turn the FET OFF.) Figure 6 illustrates the characteristics of a typical active device, as well as a modulation approach enabling extended dynamic range to be achieved. (The curves shown in Figure 6 are for a GaAs MESFET but would be similar for any FET device.) The modulation approach indicated may be applied at a single stage of the amplification chain, such at the final stage. More preferably, drain modulation is performed at the final stage, and drive modulation is performed at the initial stage, as described presently.

Referring again to Figure 3, in the case of the final stage, the operating point is set by the power supply input V_{DD3} and by the gate voltage V_G applied from the previous stage. For a given V_G (i.e., given drive voltage), as the power supply input V_{DD3} is changed, the operating point of the of the device moves up and down the V_G curve, and the output amplitude is modulated accordingly, as a function of the changing drain current I_{DD}. This kind of modulation is indicated in Figure 6 as "Drain Modulation."

To achieve the desired wide dynamic range, another kind of modulation is also required, indicated in Figure 6 as "Drive Modulation." In particular, with the stage operating in the triode region, the output amplitude can also be changed by changing the input drive to the stage. With all stages operating with low supply voltage, all stages are in triode operation, and the output power level can be further reduced (beyond a level achievable with drain modulation alone) by reducing the input drive to the initial amplifier stage. Drain modulation is still applied to the final stage through the power supply input V_{DD3}, and at the same scaling. This manner of operation allows the output power to be further reduced, to a level of 80dB or more down from the maximum power, thus achieving the desired dynamic range.

Referring to Figure 7, a more detailed block diagram is shown of one embodiment of the communications transmitter of Figure 4. The amplification

chain 713 includes three amplifier stages as previously described. A DDS/phase control block 705 includes a phase modulator/VCO 706. An amplitude control block 707 includes circuitry for achieving both drain modulation and drive modulation in the manner of Figure 6. In particular, in the illustrated embodiment, three separate power control signals are provided by the control block 103 (not shown). One of these signals, Power Control 2, is applied in common to the power supply inputs of the stages preceding the final stage. Another one of these signals, Power Control 3, is combined with an amplitude modulation signal 711 from the control block, using a multiplier 708, to produce a power supply input 715 for the final stage. Using this arrangement, because the amplitude modulation signal 715 is independent of power control signals, non-linearity in the power control signals does not affect modulation linearity. Finally, a signal Power Control 1 sets the power of the signal 709 into the amplifier by, in this embodiment, controlling the attenuation of a variable attenuator 710.

In operation, when a comparatively high average output power is desired, the signals Power Control 2 and Power Control 3 are set to a range well beyond that illustrated in Figure 6 (e.g., more than about 3 volts), and the signal input is minimally attenuated or subjected to gain, with the result that the amplifier stages are all operated in deep compression, or switch mode. In this region, the signal input level has a negligible effect on output power. For purposes of output power control, the signal Power Control 1 could be set to zero attenuation. However, it is desirable to provide substantial reverse isolation between the amplification chain and the phase modulator/VCO (e.g., to avoid VCO pulling). If the attenuator were set to zero attenuation, no reverse isolation would be achieved. By instead setting the signal Power Control 1 so as to maintain at least some minimum attenuation, reverse isolation may be achieved. The minimum attenuation is not so great as to prevent switch mode operation from being achieved. Amplitude modulation is applied solely through the amplitude modulation signal.

When a comparatively low average output power is desired, the signals Power Control 2 and Power Control 3 are set to within the range illustrated in Figure 6 (e.g., a few or several tenths of a volt), with the result that, with the gate bias values shown, the amplifier stages are all operated in triode mode. In this region the signal input level has a substantial effect on output power. The signal Power Control 1 is used to apply drive modulation after the manner of Figure 6. This effects an additional control on average output power, independent of any amplitude modulation, which is still applied through the amplitude modulation signal.

For very low power signals, the drive signal will be strongly attenuated, the degree of attenuation being reduced as desired signal power increases, until some minimum attenuation level is encountered. As desired signal power further increases, the signals Power Control 2 and Power Control 3 are increased so as to resume switch mode operation.

Referring to Figure 8, another embodiment of the communications transmitter is shown, similar to that of Figure 7. In this embodiment, an amplification chain 800 includes multiple cascaded VGA stages (803, 805, 807) followed by a final switch-mode power amplifier stage (SMPA) 809 that, except for very low output powers, remains in switch mode. A modulation generator 811 produces power control signals for each stage, including the VGA stages, which may be operated to have either positive gain or negative gain (i.e., attenuation), and the SMPA stage. A multiplier 813 is provided that receives an envelope signal and a power control signal for the SMPA stage from the modulation generator, forms the product, and applies the resulting signal as the power supply to the SMPA. The power control signals for the VGA stages, in particular, are used to control the output power at very low power levels. For switch mode power control at moderate and high power levels, all of the power control signals play an active role with the exception of the power control signal for the initial stage, used more particularly for very low power control.

A PM signal generator 815 receives modulation information from the modulation generator and a carrier signal and generates phase modulated output signal, which is applied to an RF input of the amplification chain.

The technical basis of the present invention may be further appreciated from the following description with reference to Figure 10 through Figure 16.

The approach followed, as previously described, entails switch-mode operation at high and medium output power, and conversion to "multiplicative mode" at low output powers.

Referring to Figure 10, the characteristic curves of a MESFET transistor are shown. (Other FET devices exhibit similar characteristics.) Beyond a certain drive voltage, the transistor is saturated and sources a maximum amount of current, I_{DSS}, for existing load conditions. At relatively low values of VDS, the current I_{DSS} is proportional to VDS in accordance with a proportionality constant $R_{DS,\ on}$. At increasingly higher values of VDS, the current I_{DSS} drops off by an increasing amount.

The operating space may be separated into two regions, a saturation region in which a change in drive voltage produces a proportional change in current, and a "triode region" in which this proportional relationship no longer holds.

During high power operation, the switching transistor is always driven hard, in switch mode. Hence, the transistor "snaps" between two operating points, an ON operating point at I_{DSS}, near $R_{DS,\ on}$, and an OFF operating point beyond the threshold voltage V_T, causing the transistor to enter cutoff. A line joining these two points is analogous to a conventional load line; note, however, that at high power, the transistor is not operated anywhere except at the endpoints for any appreciable portion of time. Through the mechanism of drain modulation, previously described, the voltage VDS may be controlled. As a result, the load line may be shifted, with the transistor still being operated in switch mode.

This manner of operation may be contrasted with that of conventional

amplifiers. In conventional amplifiers, as illustrated in Figure 11, the transistor is operates along a load line about a bias point defined by a bias curve. With no applied drive signal, the amplifier operates at the intersection of the load line and the bias curve. Positive drive causes the operating point the move up the load line, and negative drive causes the operating point to move down along the load line. There is not snapping between two operating points as in Figure 10. Efficiency may be improved using power-tracking methods in which the power supply voltage is reduced as the average output power is reduced. However, if the power supply voltage is reduced to a degree that the device enters the triode region (as shown), potentially serious signal distortion results.

Figure 12 and Figure 13 show magnified views of curves of Figure 10, closer in toward the origin. Referring to Figure 12, at moderately low power, a similar manner of operation as in Figure 10 is followed. To reduce feedthrough effects, the drive signal is reduced, preferably to a level just sufficient to maintain switch mode. However, feedthrough effects still set a lower limit on the achievable average output power. Achieving average output power below this lower limit requires a different operating mechanism.

Such an operating mechanism is illustrated in Figure 13. By reducing the input drive to stay above cutoff, the operating point that in prior figures corresponded to cutoff is now pushed in along the load line, into the "deep-triode" region. Operation of the device is no longer confined to the endpoints. Rather, the operating point of the device is moved along the load line by modulation of the drive signal (i.e., modulation of VGS). Furthermore, the load line may be shifted toward or away from the origin using drain modulation (i.e., changing VDS). This mode of operation is referred to herein as "multiplicative mode," since the device output is proportional to the product of the drive voltage and the drain voltage. Changing VDS effects amplitude modulation since, as the load line is shifted toward or away from the origin, the curves grow farther apart or closer together.

Changing VGS effects power control by increasing or decreasing the drain current ID.

By changing the bias level, the device may be caused to operate across a different subset of curves either closer to or farther away from $R_{DS,\ on}$. The multiplicative action of the device exhibits greater linearity and lower gain when the device is operated closer to $R_{DS,\ on}$. Figure 14, for example, shows a 5% linearity region within which the multiplicative action of the device exhibits linearity within 5%. The current through the device, ID, is only weakly affected by changes in bias, implying good temperature stability characteristics.

The multiplicative nature of device operation in the deep-triode region follows from well-established device models. While these models chosen are specific to a certain kind of devices, it should be understood that many different kinds of devices exhibit similar behavior and may be used in connection with the present invention. Triode tube devices could be used, for example, which have only a triode region and no saturation region. Hence, the following mathematical description is exemplary only.

For FETs, device operation in the saturation region and in the triode region, respectively, is described by the following equations:

$$I_D = K(V_{GS} - V_T)^2;$$
$$I_D = K(2(V_{GS} - V_T)V_{DS} - V_{DS}^2),$$

where

$$K = \frac{I_{DSS}}{V_T^2}$$

The boundary between the saturation and triode regions is defined by the simultaneous equations

$$V_{DS} = V_{GS} - V_T$$
$$I_D = KV_{DS}^2$$

In the deep-triode region $V_{DS} << V_{GS} - V_T$, resulting in

$$I_D = 2K(V_{GS} - V_T)V_{DS}$$
$$= 2K(V_{GS}V_{DS} - V_TV_{DS})$$

Hence,

$$I_D(t) = 2K(V_{GS}(t)V_{DS}(t) - V_TV_{DS}(t))$$

The last term of the expansion may be considered a bias term $V_b(t)$; i.e., it varies at the envelope frequency (typically much less than 10MHz, as compared to the RF frequency of 1-2GHz). By taking $2KV_{DS}(t) = G(t)$, the latter equation may be rewritten as:

$$I_D = G(t)V_{GS}(t) + V_b(t)$$

The bias term is readily filtered out, using an output coupling capacitor, for example, leaving the product of the envelope modulation signal G(t) and the drive modulation (power control) signal $V_{GS}(t)$.

Various methods may be used to control the transition between triode mode and switch mode in a smooth, glitch-free manner.

In one embodiment, a particular average power threshold, say -5 dBm, is identified (e.g., empirically determined). For average power levels above this threshold, the amplifier is operated in normal "switched-mode". For average power levels below this threshold, the various stages of the power amplifier are operated at conditions suitable for achieving the threshold power output; reduction of the average power below the threshold level requires only reducing the RF signal input level (e.g., by increasing the attenuation between the phase modulator and the first stage of the power amplifier). In this way, there are clearly no glitches as the attenuation can be smoothly controlled; however, there is a potential for nonlinear power steps in that a 5 dB increase in attenuation, for example, may not result in a 5 dB decrease in average output power when operating close to the threshold. Far below the threshold the threshold the output power versus attenuation curve is very linear, but close to the threshold the output power versus attenuation curve is somewhat compressed. This compression needs to be pre-corrected for in the choice of attenuation applied to arrive at a particular power level. Such

adjustment is easily accomplished.

Another embodiment avoids the need for such adjustment, as follows. When operating below the threshold, the various stages of the power amplifier are not operated at the threshold conditions but instead are operated at conditions appropriate for a higher power level (e.g., if the threshold is -5 dBm, the power amplifier stages are operated as if the desired power level was, say 0 dBm). The attenuation before the first stage of the power amplifier must be greater this way, but the greater attenuation substantially avoids the nonlinear relationship between an attenuation step and the resulting step in output power when output power is close to the threshold. Determination of the attenuation setting to be used for the power level immediately below the threshold may be easily accomplished by one skilled in the art of RF measurements. Once this value is set, lower power levels may be achieved in linear dB steps through linear dB steps of the attenuator.

Various other embodiments may be used to advantage. For example, in the low output power mode in which all amplifier stages are operated in triode mode, instead of applying any amplitude modulation on the final stage as described, amplitude modulation can be applied at any of the stages in the amplifier chain, including any of the stages preceding the final stage, using an appropriate amplitude modulator such as the multiplier previously described.

The desired amplitude modulation characteristic need not be applied though a single signal or single stage. Rather, the desired amplitude modulation characteristic may, if desired, be broken up into multiple amplitude modulation signals the product of which yields the desired amplitude modulation characteristic. These multiple amplitude modulation signals may be applied to any combination of the amplifier stages and the amplitude varying circuit. Furthermore, the foregoing modulation approach may be applied to any stage so long as all succeeding stages operate linearly.

Furthermore, if desired, the same amplitude modulation signal may be

applied to multiple control ports. Applying the modulation to two ports effects a squared signal modulation, applying the modulation to three ports effects a cubic signal modulation, and so forth. When the amplifier is operated in this manner, each stage effectively acts as an independent multiplier.

Referring to Figure 9, a more generalized block diagram of a communications signal amplifier is shown, embracing the foregoing variations. A carrier signal C is applied to an amplitude varying circuit 803 responsive to a power control signal $Pout_1$ to produce a carrier signal C'. The carrier signal C' is then amplified by a linear amplifier chain 813 having one or multiple stages. The power supply of at least one such stage is varied in accordance with a desired amplitude modulation characteristic. The power supply input of each individual stage may be fixed (PS), varied in accordance only with a desired output power level (Pout) or in accordance only with a desired amplitude modulation characteristic (AM), or varied in accordance with both a desired output power level and a desired amplitude modulation characteristic (Pout/AM). In some instances, power supply inputs of multiple stages may have identical AM components.

EXAMPLE

The foregoing method was applied to a demonstration board to control the average output power of a board-generated signal compliant with the EDGE specification from a maximum output power of 30 dBm down to very low output power of -50 dBm. The spectrum and error vector magnitude (EVM) of the output signal at both high power and at low power was measured. The results are shown in Figure 15 and Figure 16, respectively. Almost no spectral degration or EVM degradation is observed.

Thus, there has been described power control methods and apparatus for achieving extremely high dynamic range power control with inherent accuracy and outstanding signal fidelity over the entire dynamic range. To achieve low output

power signals, the power supply inputs of the amplifier stages are set for triode operation, at very low (possibly negative) gain. The power supply input of the final stage is amplitude modulated (using drain modulation), and the amplitude of the drive signal is adjusted in a series of steps through variable power supply voltage settings of the driver transistors and also through input attenuation (drive modulation). As a result, it becomes possible to produce output signals having average power anywhere within a wide range, or to greatly increase the dynamic range over which amplitude modulation may be produced at a given average power level, or both.

With envelope modulation applied at the final amplifier stage, modulator and amplifier noise are suppressed, with the result that the signal noise floor is limited by the noise characteristics of the frequency determining element, i.e., the VCO. Independent control of envelope power and average output power is made possible, which, although not required, allows the envelope insertion procedure to have fixed scaling, independent of output level. In any event, no variation of the output network (load line) is required. Furthermore, no triode distortion occurs as in known power-tracking methods.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.